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# In place growth of vertical Si nanowires for surround gated MOSFETs with self aligned contact formation

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**Abstract** – We demonstrate the simultaneous vertical integration of self contacting and highly oriented nanowires (NWs) into airbridge structures which have been developed into surround gated metal oxide semiconductor field effect transistors (MOSFET). Such vertical NW architecture can be easily integrated into existing ICs processes opening the path to a new generation of nonconventional nano devices. To demonstrate the potential of this method surround gated vertical MOSFETs have been fabricated with a highly simplified integration scheme combining top-down and bottom-up approaches, but in the same way one can think about the realization of integrated nano sensors on the industrial scale.

We show a nanodevice fabrication method which is based on the combination of a bottom up method and conventional top down ICs manufacturing techniques. The vapour-liquid-solid (VLS) approach provides the epitaxial growth of vertical Si-NWs from individual Au catalysts and allows us to control the nanowire location and its orientation and thereby their alignment to the prepatterned nanoarchitecture. NWs are grown where the device is fabricated. Our method is scalable, i.e., this could be done on 300mm wafers and one can make many of them. We show that suspended nanowire architectures can be developed into surround gated MOSFETs (Figure1). In the demonstrated device, unintentionally p-doped Si-NWs grown epitaxially on a p-doped substrate were used as active channel material. These first-generation, unoptimized devices already show gate-voltage-dependent current increase of more than 3 orders of magnitude (Figure 2).
This technique in combination with other nanofabrication methods due to its scalability and ease of device fabrication, goes beyond the current state-of-the-art assembly of NW based devices such as transistors and sensors and may be used as a platform for building more complex architectures such as hierarchical 3D modules. Such three-dimensional device architecture could further increase the transistor density through the additional ability to integrate multiple gates and source/drain connections along the length of these high aspect ratio channels. Although the nanowires were grown with Au colloids, similar results have been achieved using semiconductor industry-friendly catalyst compositions such as Pt, Ti or Al.[i, ii]
The ability to synthesize longitudinal and coaxial heterostructures of NWs will allow additional design flexibility.

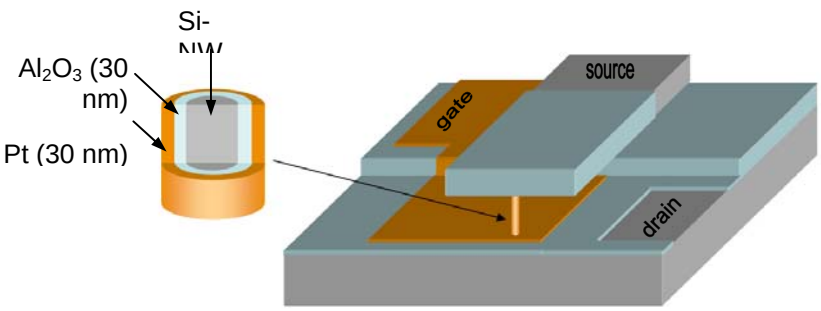


**Figure 1:** Schematic of the surround gated Si-NW FET structure. The channel of the FET is generated via VLS Si-NW synthesis with self-aligned contact formation. Gate dielectric and metal formation was completed by first depositing a 30 nm thick $Al_2O_3$ layer on the entire device using ALD. The Pt wrapped around gate electrode was deposited again by ALD.

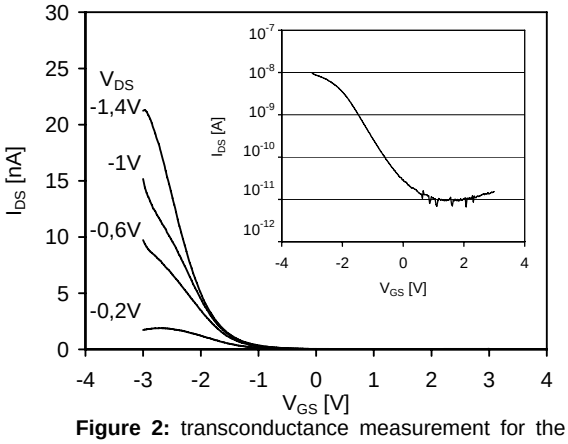


**Figure 2:** transconductance measurement for the vertical surround gated NW FET. The inset in Figure 5b shows the semilog plot of the full $I_{DS}$ vs. $V_{GS}$ spectrum at $V_{DS}$= -1V.

**References**

[i] Sharma, S.; Kamins, T. I.; Williams, R. S. J. Cryst. Growth **2004**, 267, 613.
[ii] Wang, Y.; Schmidt, V.; Senz, S.; Gösele, U. Nature Nanotechnology **2006**, 1, 186.