

11<sup>th</sup> International Conference on Advanced Materials

Rio de Janeiro Brazil September 20 - 25

Compliant Organic Thin Film Transistors on Elastomeric Substrates

## S. P. Lacour<sup>(1)\*</sup>, I. M. Graz<sup>(1)</sup>

- (1) Nanoscience Centre, Department of Engineering, University of Cambridge, 11 JJ Thomson Avenue, Cambridge CB30FF, UK, <u>spl37@cam.ac.uk</u>, <u>img21@cam.ac.uk</u>.
- \* Corresponding author.

**Abstract** – We have fabricated top contact pentacene OTFTs on elastic silicone substrate. The devices are prepared using shadow masking and an all-vapour phase process. Electrodes are made of thin gold films and the gate dielectric is a layer of parylene C. The pentacene OTFTs on PDMS have acceptable levels of performance with threshold voltage of  $V_{th} \sim -10V$ , mobility of up to  $0.3 \text{cm}^2/\text{V.s}$  and on/off ratio of  $5.10^4$ . Active load inverters made of two pentacene OTFTs interconnected with stretchable gold conductors have a maximum gain of 2.5, and can reversibly bend over the wrist.

Organic electronics based on evaporated small molecules such as pentacene offer a number of attractive features such as dry and room temperature processing to prepare electronic circuits on elastomer. In this paper, we report on the successful fabrication and characterization of pentacene OTFTs made directly onto PDMS substrate using an all-vapour phase process flow and shadow mask patterning.

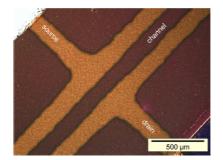
The OTFTs on PDMS are prepared in a bottom up approach similarly to OTFTs on plastic foils. The transistors have a bottom gate and co-planar top source/drain architecture. First smooth PDMS membranes are prepared by spin-coating onto silicon wafer or casting, and cured at 60°C for 12h. The OTFTs are fabricated in 4 steps using 3 shadow masks: gate evaporation (chromium/gold films, 5nm/50nm thick), gate dielectric coating (parylene C, 200nm thick), pentacene (50nm thick) and source/drain (gold, 30nm thick) evaporations. After fabrication, the OTFTs on PDMS are characterized in a glove box with an Agilent parameter analyzer.

A microscopic picture of the OTFT on PDMS is shown figure 1. The channel is  $100\mu m$  long and  $3000\mu m$  wide. There are no cracks across the films but random buckling cover the channel and the top electrodes. In the channel, we measured an average pentacene grain size of 50-100nm within the wrinkled film.

Transfer and output characteristics of an OTFT on PDMS are shown Figure 2. The threshold voltage is ~-9V, the on/off ration is  $5x10^4$ , and a saturation mobility of about 0.3 cm<sup>2</sup>/V.s, which is comparable to that of pentacene films evaporated on plastic substrates [1]. Active load inverters were also prepared on PDMS with two OTFTs ( $W_1/L_1 = 2$ , and  $W_2/L_2 = 6.7$ ) interconnected with stretchable metallization [2]. The circuits switch at about  $V_{in} = -10V$  and have an initial gain of 2.5. Then the circuits on PDMS were bent over a 7cm radius pipe for 1min and relaxed. They did not fail. However their performance slightly degraded with switching voltage and gain decreasing to -12V and ~1.

We have demonstrated that pentacene OTFT process is compatible with elastic silicone substrates. This is an important result towards the fabrication in a bottom-up approach of large area and elastic electronic circuits onto stretchable substrates.

This work is sponsored by the Royal Society and the collaboration on Nanoscience between Nokia and the University of Cambridge.

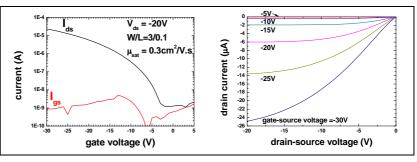


**Figure 1:** Top view of a pentacene OTFT (bottom gate architecture) on PDMS substrate. The 10µmx10µm AFM scan illustrates the wrinkled OTFT channel stack (PDMS/Au/Parylene/Pentacene).

## References

[1] B. Street, Adv. Mat. 21 (2009) 1.

[2] I.M. Graz, S.P. Lacour, (2009), submitted.



**Figure 2:** Transfer (left) and output (right) characteristics of the coplanar pentacene OTFT on PDMS.