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Electrical Characterization of Porous Silicon on p-Si Heterojunction

M.A. Chavarria and F. Fonthal

Advanced Materials for Micro and Nanotechnology Research Group, Facultad de Ingeniería, Universidad Autónoma de Occidente, Km. 2 vía Cali - Jamundi, Valle del Lili, Cali, Colombia, e-mail: mchavarria@uao.edu.co – ffonthal@uao.edu.co

Abstract – The DC and AC electrical characterization of Au/porous silicon/p-Si/Al structure is presented. The low porosity porous silicon layers were prepared by electrochemical etching time of 180 s in p-type silicon <100> substrates. The I-V characterization were obtained in the DC range of ± 10 V and the AC electrical measurements capacitance – conductance – frequency were performed from 5 Hz to 10 MHz, at room temperature in the DC range of ± 2 V. We have obtained the parameter fitting values according an electrical model circuit in DC and AC under different resistivities of the silicon wafers.

Porous silicon (PS) is a nanostructured semiconductor material usually obtained by electrochemical anodizing of silicon wafers p-Si [1]. In order to investigate its electrical properties, the structure formed it's a diode junction (metal/PS/p-Si/metal), in type p of crystalline silicon [2]. Different conduction mechanisms have been proposed in order to explain the DC electrical behavior of such PS structures. Specifically, it has been suggested [3-5] that conduction mechanisms such as electrical transport in the silicon crystallites, Schottky rectification, Poole-Frenkel, SCLC and injection power law are the possible mechanisms for the electrical behavior of PS structures.

Measurement of AC electrical characterization is important for dielectric characterization of materials. This characterization technique permits to separate the dielectric permittivity properties corresponding to the capacitances present in the relaxation region in the porous silicon layers [5]. The AC dielectric analysis is interpreted in terms of the admittance or impedance measurement and the equivalent electrical circuits are formed by RC networks in parallel [6], connected in series with an inductance [7,8] or capacitance [5]. In conjunction with structural characterization, the various model parameter values fitting corresponding Au/PS structures fabricated completed a physical analysis in the structure studied under different fabrication processes [7].

We present the AC impedance analysis and the DC current-voltage characteristics of two Au/PS/p-Si/Al samples comparing its response according to two resistivities of the silicon wafers, at room temperature. Finally, we have found two equivalent circuits which properly fit the DC and AC experimental measures of the structures studied and the parameters that represent the conduction mechanisms as the low frequency phenomenon, the geometric capacitance and the depletion capacitances presented in the structures were determined.

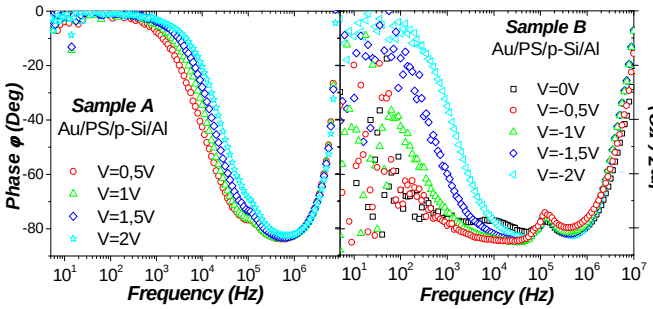

Figure 1: Phase φ (deg) vs. frequency (Hz) dependencies of the samples A and B studied for different voltages applied.

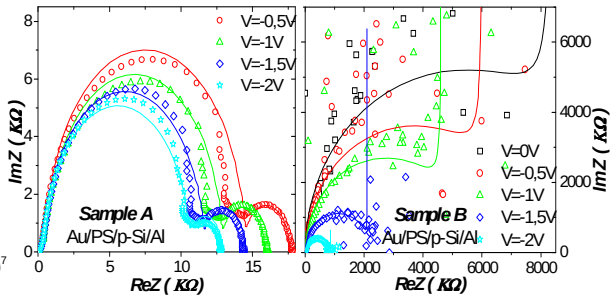

Figure 2: Cole–Cole plot Im(Z) vs Im(Z) of the samples A and B studied for different voltages applied.

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